SESSION 10 – TAPA II
Wireless Baseband

Friday, June 18, 10:20 a.m.
Chairpersons: A. Abidi, UCLA
M. Ugajin, NTT

10.1 — 10:20 a.m.
A 32 mW Self Contained OFDM Receiver ASIC for Mobile Cellular Applications, H. Zou and B. Daneshrad, University of California, Los Angeles, CA

An OFDM receiver ASIC targeting cellular terminals has been designed and fabricated in 0.18 μm CMOS. The receiver incorporates a front-end receiver, pre/post-FFT processing units, a 1024-point complex (I)FFT processor, a channel estimator and corrector, all digital synchronization loops, and a control and configuration interface. Low power circuit techniques and system algorithm optimization lead to the final receiver ASIC that dissipates only 32mW while providing a (uncoded) date-rate of 8.192 Mb/s, making the chip suitable for packet-based mobile applications.

10.2 — 10:45 a.m.
A CMOS 64MSps 20mA 0.85mm^2 Baseband I/Q Modulator Performing 13 bits over 2MHz Bandwidth, C. Pinna, A. Mecchia and G. Nicollini, STMicroelectronics, Milan, Italy

A CMOS 64MSps 2-1-1 cascaded sigmadelta I/Q modulator optimized for WCDMA applications achieves more than 13 bits over 2MHz bandwidth. A new way for sizing cascaded sigma delta architectures based on comparator equivalent gain, and an improved dynamic element matching method resulted into an area and power efficient modulator design. The total consumption of two modulators plus built-in reference generators is about 20mA at 2.7V. Total active area is 0.85mm2 in a 0.35um CMOS technology.

10.3 — 11:10 a.m.
A COFDM Baseband Processor with Robust Synchronization for High-Speed WLAN Applications, H.-Y. Liu, Y.-H. Yu, C.-C. Lin, C.-C. Chung, T.-Y. Hsu and C.-Y. Lee, National Chiao Tung University, Hsinchu, Taiwan, ROC

A high-performance and low-cost COFDM base band processor is presented. With algorithm exploration in channel estimation and phase error tracking, synchronization becomes more robust to enhance system performance. And better design SNR (1.35~7.16dB) can be achieved compared to current solutions. Through architectural exploration, the proposed base band processor designed in 0.18um CMOS process contains only 370K logic gates and 3.3K byte memory. Measurement results show that better hardware efficiency and performance enhancement is achieved for high-speed WLAN applications.

10.4 — 11:35 a.m.
An Area-Efficient Implementation of Digital-IF QAM Coherent Demodulator for Software-Defined Radio Receivers, Y. Song, J. Kim and B. Kim, Korea Advanced Institute of Science and Technology, Daejeon, R.O. Korea

This paper presents a digital-IF QAM coherent demodulator implemented on 0.11-mm2 die area. Two independent resampling circuits with second-order digital tracking loops are employed in order to achieve both the carrier and timing recoveries. A coherent demodulator with complete digital synchronization functions achieves a bit-error rate of 10^-6 with an implementation loss of 0.6dB for uncoded 16-QAM signal. It consumes 16 mW with a 1.8-V supply, working in 80 MHz.

Lunch 12:00 pm